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Temperature Monitoring Circuitry Design for the Uncooled Focal Plane Arrays Infra-Red Sensor

Yan Wang,
[1] *(School of Electronic and Information Engineering, Tianjin Polytechnic University, China)*

Abstract: *Temperature monitoring circuitry design for the uncooled focal plane arrays infra-red sensor is presented. An uncooled infrared array detector system and temperature detection circuit system is proposed in this dissertation. In this system, the core modules include temperature detection circuit, level converter, NOT gate and NAND gate. A top-down design approach is used in this dissertation.*
Keywords: *Uncooled infrared detector, temperature detection circuit, a top-down design approach*

I. Introduction

The infrared ray that is produced by the vibration and rotation of the molecules is an electromagnetic wave. In the nature, all objects (above absolute zero) generate infrared radiation. Volatility is expressed as polarization, interference and diffraction. The particle of infrared radiation is in the form of photon absorption and emission. The purpose of infrared detection is using photoelectric conversion to process the received radiation (target and background), and changing the temperature distribution of the target image into video images. Infrared detectors can be divided into refrigeration (quantum type infrared detector) and uncooled infrared detector (hot). Among them, there are very important characteristics of uncooled (hot) infrared detection system, such as simple and easy to implement, high stability and low cost.

With the rapid development of infrared technology, the application of temperature sensor is more extensive and universal. Since the object that is higher than the absolute zero (due to internal thermal motion) will be emitted around the radiation electromagnetic waves. Infrared temperature sensor is produced by the use of this principle. Infrared temperature sensor has the advantages of convenient installation, simple measurement, high accuracy, high sensitivity and high Signal-to-Noise Ratio, so it is widely used in daily life.

In this paper, the structure of temperature detection circuit is presented. The details of its structure and circuit will be described in the next section. The second part describes the functions of temperature sensor circuit. The third parts are simulation results. The fourth part is the conclusion.

II. System overview

The system overview of the temperature detection is shown in fig.1. It can be divided into four parts, including temperature detection module, Levelshift converter, NAND gate and invertor. The temperature detection module is composed of five parts, including the circuit, the buffer circuit, the switch, TRIM_RES1 and TRIM_RES2.

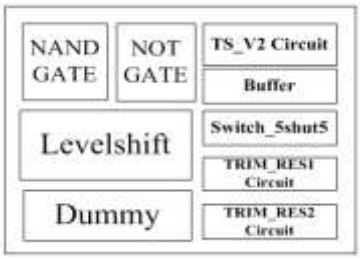

Fig.1 the system overview of the temperature detection

The input pin and the output pin are placed on the left and right side of the chip. As shown in the fig.2. The top and left of the chip are the power supply pin.

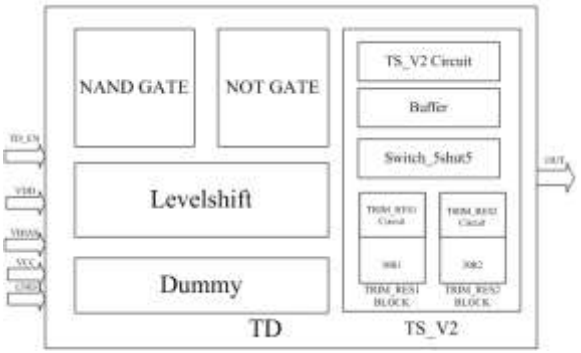

Fig.2 the input and the output of the temperature detection

III. Functional description and introduction

Temperature detection circuit is used to detect chip temperature. When the chip temperature is higher than 85℃or lower than -40℃, it will produce a warning signal. When the chip is in normal temperature, it will not produce an alarm signal.

When the chip is powered, it reset firstly, and its internal reference source start to work, after the resetting, it will enter the test state. The test results will be output in less than 15μs after the chip powered(not including the establishment of VBG time). It can be stable in the detection of the output stability. If the chip temperature is lower than -40℃ or higher than 80℃, the alarm signal will be generated. The two state including open and close can be chosen. In the close state, the power consumption will be very low. It can output of high or low temperature detection results. In the design process, considering the electrostatic discharge (ESD) problem, the product's life and the stability and safety of the product.

The TS_V2 chip integrated with the buffer circuit, switch, TS_V2 circuit, TRIM_RES1 and TRIM_RES2 modules and other components. The left and right sides of the Dummy circuit are connected to the VCC, it can not be ignored in the layout design. The layout of the chip is not only to test the logic function of the circuit, but also to ensure that the LVS is correct.

Dummy can reduce the technologic errors. The purpose of the buffer circuit is to reduce the internal device over current or over voltage and reduce the switching losses of the device. Switching losses are easy to heat and damage the device, using this circuit can improve the working condition of the circuit. The switch circuit is composed of two PMOS. The TRIM_RES1 module is composed of invertor, 30R1 and NMOS.

CMOS invertor circuit is composed of two enhanced MOS, the below of the tube is NMOS, called the drive pipe, and at the top of the tube is PMOS, called load tube[1]. The NMOS tube has a positive gate open voltage (UTN), and the PMOS tube has a negative gate open voltage (UTP), and the numerical range is between 2V and 5V[2]. In order to guarantee the normal operation of the circuit, the power supply voltage must satisfy the following equation1.

$$UDD > (UTN+|UTP|) \quad (1)$$

The TRIM_RES2 module is similar to the schematic of the TRIM_RES1 module. It is made up of non-gate and NMOS. The main differences are reflected in the 30R2.

The three input NAND gate circuit consists of three parallel PMOS and NMOS tube[3]. Each of the three inputs (A1, A2, A3) is connected to a PMOS tube and a NMOS transistor. When the input is in high level, three NMOS conduction and three PMOS cutoff, the output is low level. When at least one of the three input is low, at least one of the three parallel PMOS is conducting, and at least one of three series of NMOS is cutoff, the output is high level[4], thus realizing the function of three input NAND gate.

The using of the level conversion circuit is to solve the problem that the logic of internal input and output is not coordinated[5]. The problem is due to the introduction of voltage logic. In order to maintain the stability of the system, this problem should be considered in the design system.

IV. Simulation

The temperature detection circuit is realized in 0.35μm CMOS process. The power supply voltage is 4.5V, 5.0V, 5.5V, and the process condition is MOS (TT, SS, FF, NSPF, NFPS), CAP (TT, SS, FF), RES (TT, SS, FF). The simulation results of temperature detection circuit are shown in fig.3. It is the top circuit diagram. All of the following simulation results are based on this circuit diagram.

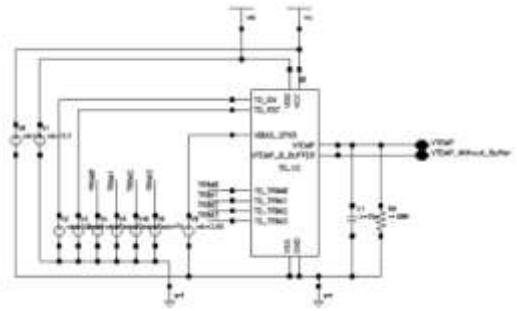

Fig.3 the temperature detection circuit diagram

In the temperature range of -20℃ to 80℃, the simulation result of the transconductance of the whole circuit is simulated. The simulation result is shown in Fig.4.

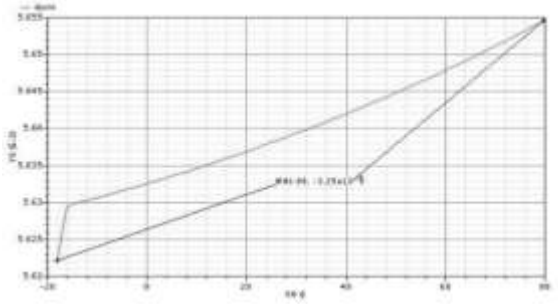

Fig.4 the relation of the transconductance and temperature

When the frequency is 1 Hz to 10^9 Hz, the simulation result of the PSRR (power supply voltage suppression ratio) of the entire circuit is simulated. The simulation result is shown in the following Fig.5.

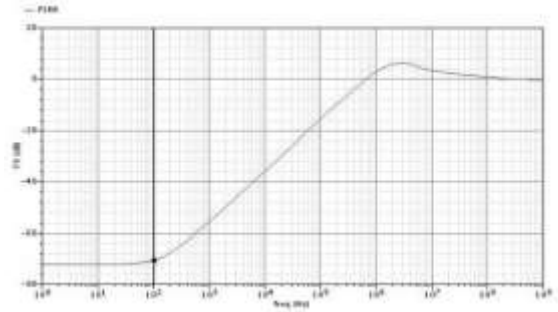

Fig.5 The relation of PSRR and frequency

When the frequency is 1 Hz to 10^9 Hz, the voltage of the absolute temperature (VPTAT) is simulated under the AC response. The simulation result is shown in fig.6.

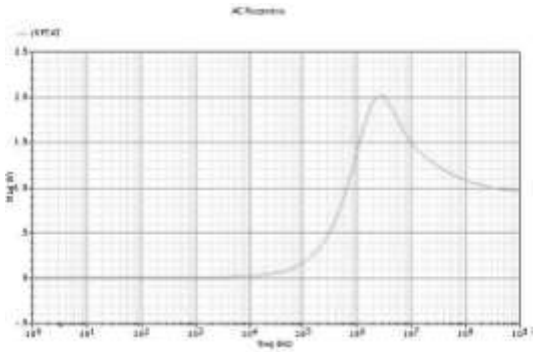

Fig.6 the relation of VTPAT and frequency under the AC response

In the temperature range of -25℃ to 100℃, the voltage of the absolute temperature (VPTAT) is simulated under the direct current response. The simulation result is shown in Fig.7.

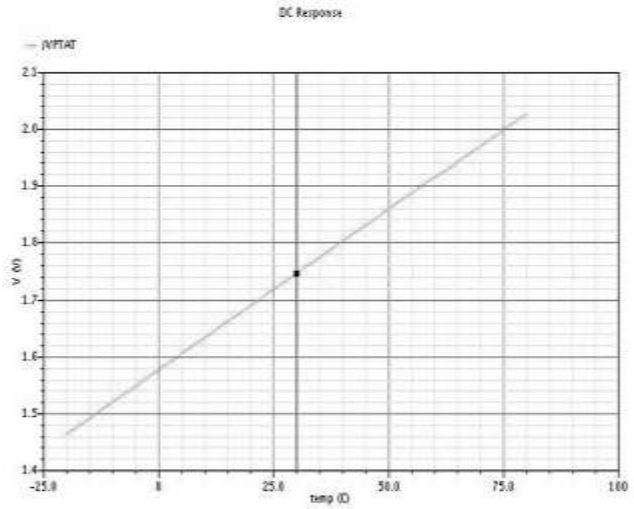

Fig.7 the relation of the VTPAT and temperature under the DC response

V. Conclusion

The chip of temperature detection circuit is presented. It is realized in 0.35μm CMOS process. The power supply voltage of the chip is 3.3V. The chip area is 0.6mm x 0.6mm excluding pads. The temperature detection circuit has good performance and stability. It satisfies the needs of industrial requirements.

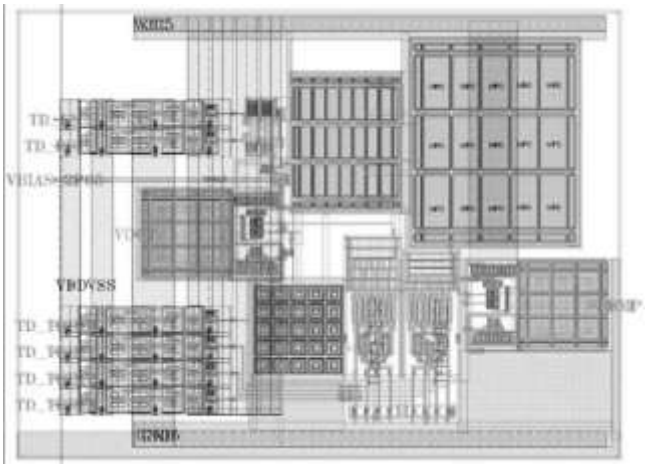

Fig.8 complete layout of the temperature detection circuit

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